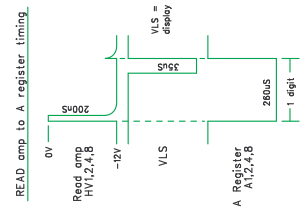


L0 SPE only clears the MD, MR and ACO registers

- READ-BUSS [3]
- DIGIT-BUSS [3,4,9,12]
- CORE-BUSS [2]
- A-BUSS [3,4,6,7,8,9]
- C-BUSS [2,3,4]
- CONTROL [2,3,4,5,6,7,8,9,10,11]



Each of these eight groups of ROW / COLUMN wire sets is shown passing through one plane only. They actually pass through all four planes.

RevNo	Revision note	Date	By	Checked

1	2	3	4	5	6	7	8	9	10
A	B	C	D	E	F	G	H	J	K

Pcb Dwg # =	Name	Date	Title
	MD Hatch	21/10/2009	Soemtron ETR 220 Calculator #1 - Core Memory Logic Diagram
Scale	Nts	Sheet	
		1	
		Next Sheet	2
		Drawing Number	Soemtron 220 Logic
			A2
			Issue
			A

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