

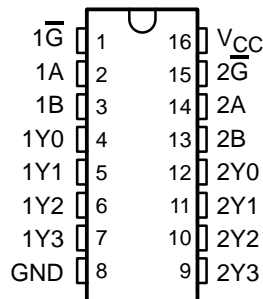
SN54HC139, SN74HC139

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

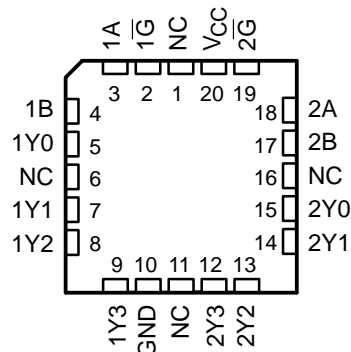
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- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

SN54HC139 . . . J OR W PACKAGE
SN74HC139 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC139 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HC139 are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The 'HC139 comprise two individual 2-line to 4-line decoders in a single package. The active-low enable (\overline{G}) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54HC139 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC139 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

\overline{G}	INPUTS		OUTPUTS			
	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

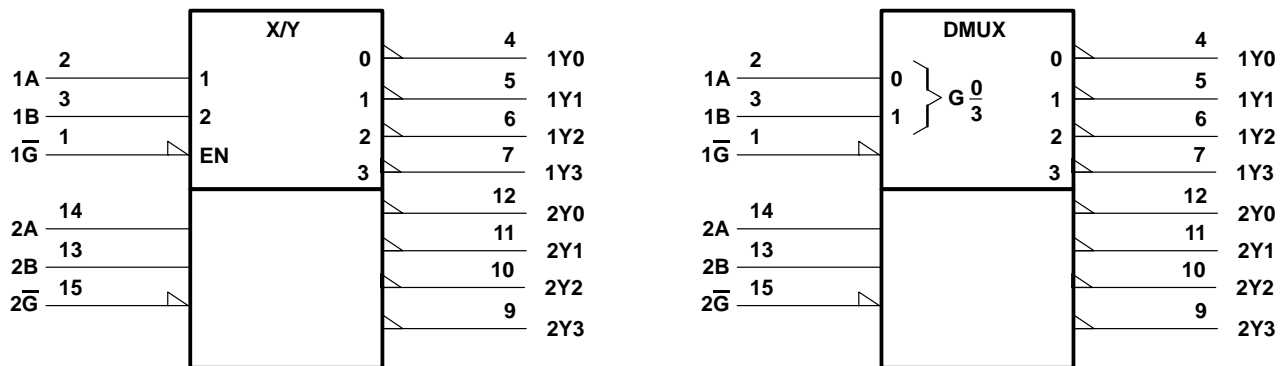
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SN54HC139, SN74HC139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

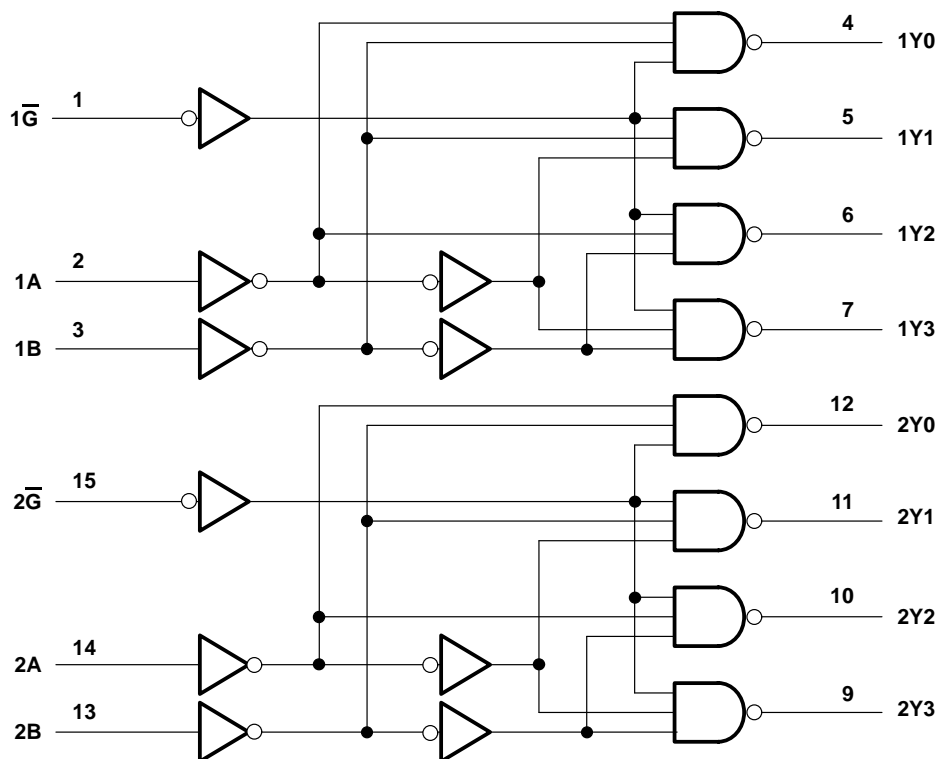
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logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

SN54HC139, SN74HC139

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC}	–0.5 V to 7 V	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA	
Continuous current through V_{CC} or GND	±50 mA	
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	D package	1.3 W
	N package	1.1 W
	PW package	0.5 W
Storage temperature range, T_{stg}	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

		SN54HC139			SN74HC139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$		1.5	$V_{CC} = 2\text{ V}$		1.5	V
		$V_{CC} = 4.5\text{ V}$		3.15	$V_{CC} = 4.5\text{ V}$		3.15	
		$V_{CC} = 6\text{ V}$		4.2	$V_{CC} = 6\text{ V}$		4.2	
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0	0.5	$V_{CC} = 2\text{ V}$		V
		$V_{CC} = 4.5\text{ V}$		0	1.35	$V_{CC} = 4.5\text{ V}$		
		$V_{CC} = 6\text{ V}$		0	1.8	$V_{CC} = 6\text{ V}$		
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) time	$V_{CC} = 2\text{ V}$		0	1000	$V_{CC} = 2\text{ V}$		ns
		$V_{CC} = 4.5\text{ V}$		0	500	$V_{CC} = 4.5\text{ V}$		
		$V_{CC} = 6\text{ V}$		0	400	$V_{CC} = 6\text{ V}$		
T_A	Operating free-air temperature	–55	125		–40	85		°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC139		SN74HC139		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V		
			4.5 V	4.4	4.499		4.4		4.4			
			6 V	5.9	5.999		5.9		5.9			
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7		3.84			
		I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2		5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V	
			4.5 V		0.001	0.1		0.1		0.1		
			6 V		0.001	0.1		0.1		0.1		
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33		
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33		
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V					8		160	80	μA
C _i			2 V to 6 V			3	10			10	10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

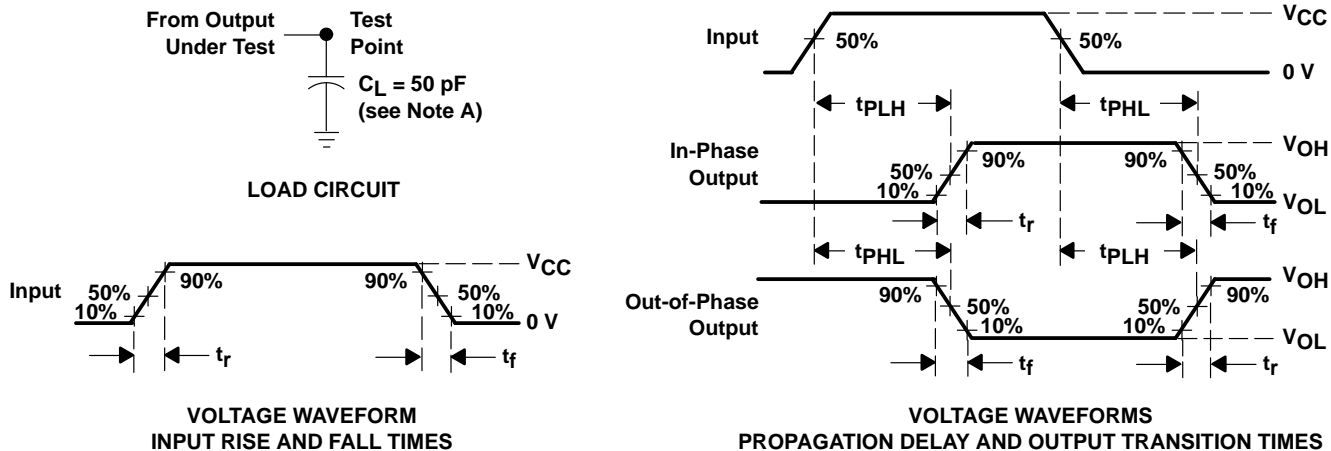
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC139		SN74HC139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	2 V		47	175		255		220	ns
			4.5 V		14	35		51		44	
			6 V		12	30		44		38	
	Ḡ	Y	2 V		39	175		255		220	
			4.5 V		11	35		51		44	
			6 V		10	30		44		38	
t _t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per decoder	No load	25	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 C. The outputs are measured one at a time with one input transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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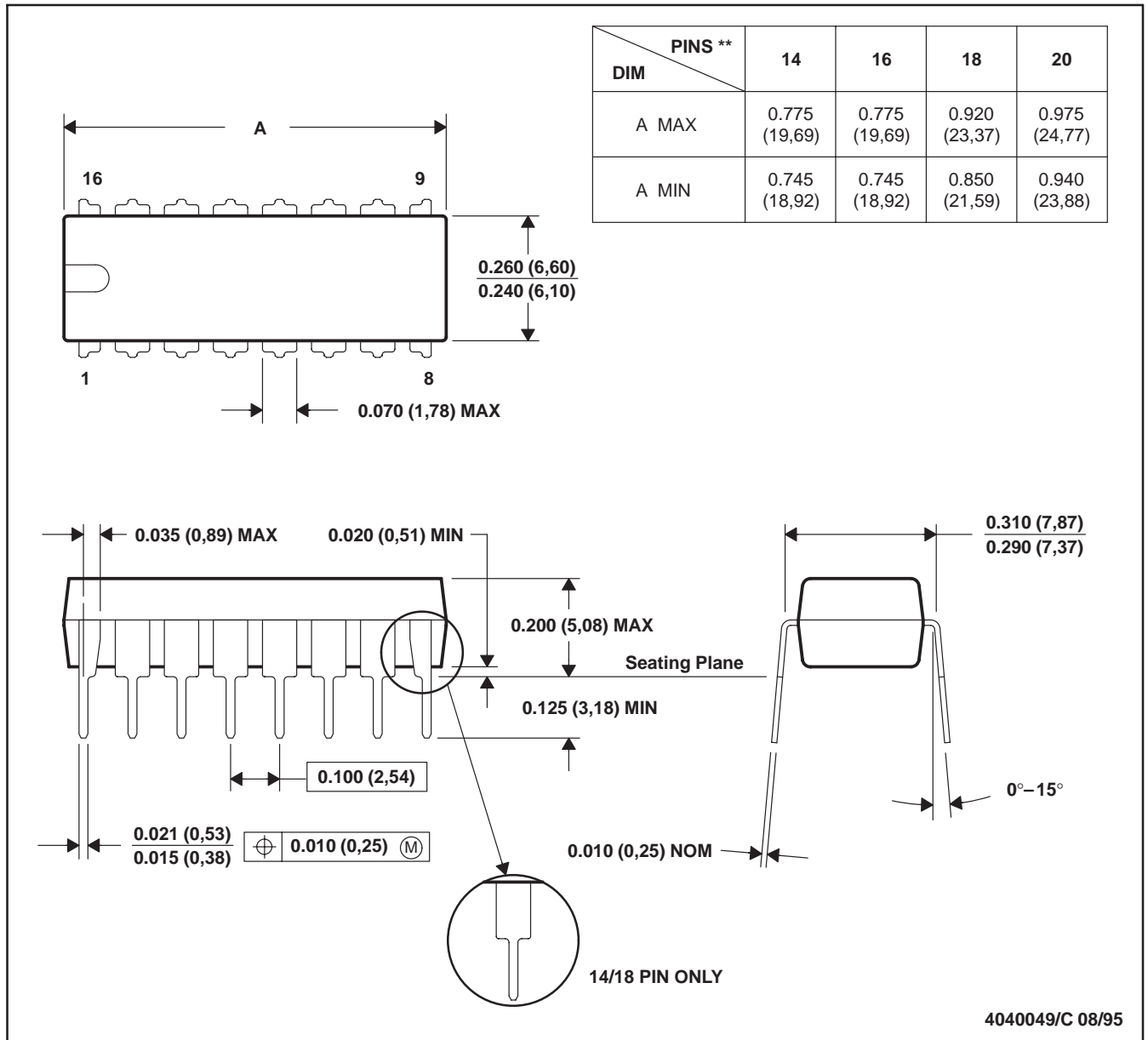
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N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).