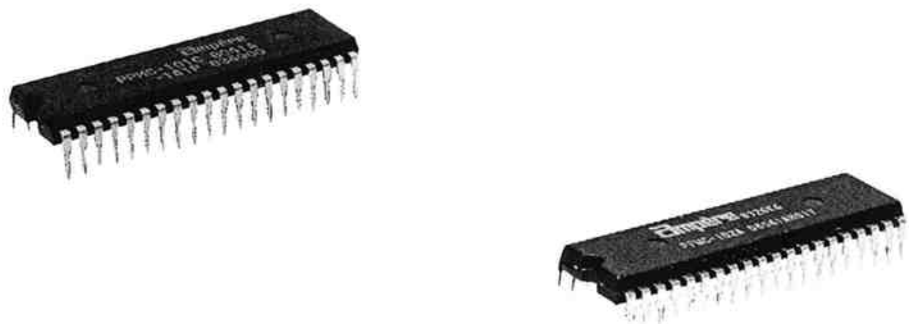
# STEPPER MOTOR CONTROL LSI

# PPMC 101C/102A

## DATA MANUAL



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# INTRODUCTION

*PPMC101C/102A is a unique one-chip LSI specially designed to interface a stepper motor to an 8-bit micro computer with no additional hardware. PPMC101C/102A provides 8 kinds of different operations by the command of master CPU including acceleration/deceleration and constant speed operation.*

*Operating frequency and number of phase for stepper motor are programmable. Distribution signal to excitation driving circuit can also be programmble for selection of 2-phase or 1-2 phase excitation (2-3 phase excitation for 5-phase motor) for 3, 4 and 5 phase motor.*

*In addition, PPMC101C/102A provides five kinds of "limit" switch input. Complete function necessary to control stepper motor is included in one chip LSI. The PPMC101C/102A can be easily interfaced with a microcomputer system.*

## 1. PPMC101C/102A SPECIFICATIONS

*Operation Command*

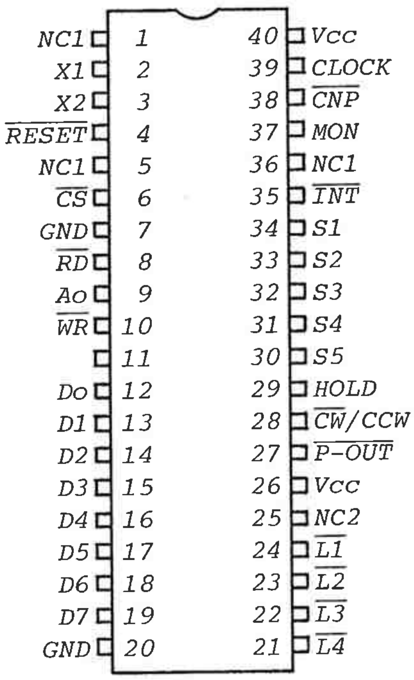
* *Emergency Stop*
* *Decelerating Stop*
* *Single Step*
* *Acceleration & Deceleration*
* *Constant Speed Operation*
* *To move to the "Limit"*
    - *(1) To move to the high speed limit*
    - *(2) To move to the base point*

*Excitation Method*

| *Motor* | *Excitation* |
|---|---|
| *3-phase* | *2 phase* |
| | *1-2 phase* |
| *4-phase* | *2 phase* |
| | *1-2 phase* |
| *5-phase* | *2 phase* |
| | *2-3 phase* |

| | | |
|---|---|---|
| Number of steps | : | 16,777,216 max |
| Number of pulse for acceleration/deceleration | : | 4 - 8,160 |
| Maximum pulse rate | : | PPMC101C ... 5K pps (RA=20, fo=100KHz)<br>PPMC102A ... 10K pps (RA=20, fo=200KHz) |
| Power supply | : | 5V ± 5%   125mA max |

## 2. TERMINAL ASSIGNMENT AND FUNCTIONS




(Top View)

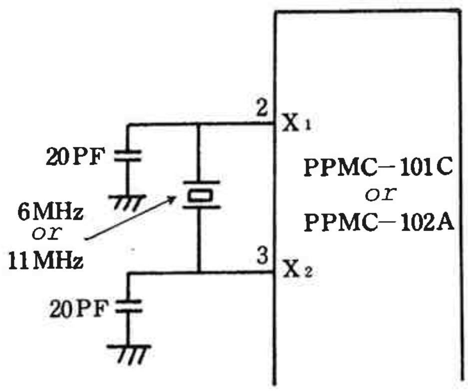
40 pin Dual-In-Line

| Signal | Pin# | I/O | Description |
|---|---|---|---|
| X1, X2 | 2, 3 | I | X-tal |
| RESET | 4 | I | RESET input |
| CS | 6 | I | Chip Select |
| RD | 8 | I | READ strobe |
| Ao | 9 | I | Address 0 |
| WR | 10 | I | WRITE strobe |
| SYNC | 11 | O | Timing output |
| Do - D7 | 12-19 | I/O | Data Bus 8-bit |
| L4 | 21 | I | Reverse high speed limit input |
| L3 | 22 | I | Forward " " " " |
| L2 | 23 | I | Reverse limit input |
| L1 | 24 | I | Forward " " |
| P-OUT | 27 | O | Pulse output |
| CCW/CW | 28 | O | Forward/Reverse status<br>'0' = Forward<br>'1' = Reverse |
| HOLD | 29 | O | Motor HOLD output |
| S5 | 30 | O | Motor 5th phase output |
| S4 | 31 | O | " 4th " " |
| S3 | 32 | O | " 3rd " " |
| S2 | 33 | O | " 2nd " " |
| S1 | 34 | O | " 1st " " |
| INT | 35 | O | Interrupt signal |
| MON | 37 | I | External control<br>'0' = Motor ON<br>'1' = Motor OFF |
| CNP | 38 | I | Base point signal input |
| CLOCK | 39 | I | External clock input |
| Vcc | 26,40 | I | +5V DC |
| GND | 7,20 | I | 0 V |
| NC1 | 1,5,36 | I | pull up to Vcc with 3.3K ohm or open |
| NC2 | 25 | O | OPEN |

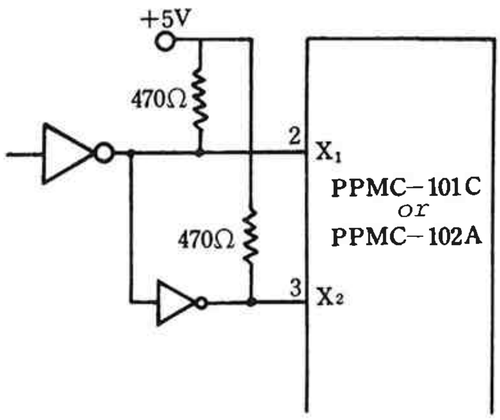
## PIN DESCRIPTION

### 2-1 X 1, X 2

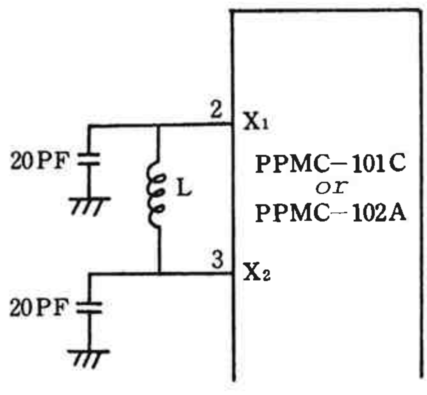
*Inputs for a crystal. PPMC101C is normally operated with a 6 MHz crystal and PPMC102A with a 11 MHz crystal. You may also drive the clock inputs with an LC turned circuit or an external clock source (2 phases) as shown in Fig 2-1. 1 to 6 MHz for PPMC101C and 1 to 11 MHz for PPMC102A can also be used for driving frequency, but the operating speed slows down in accordance with the clock frequency.*




*X-tal Clock Driver*




*1 - 6 MHz Input Frequency*
*External Clock Driver Circuit*




*LC Turned Circuit Clock Driver*

*Fig 2-1*

| PPMC−101C | | PPMC−102A | |
|---|---|---|---|
| L=130 μH | 3 MHz | L=120 μH | 3.2 MHz |
| L= 40 μH | 5 MHz | L= 45 μH | 5.2 MHz |

## 2-2 $\overline{\text{RESET}}$

*Input used to reset status flip-flops and to set the program counter to zero. This pin should be connected to the RESET signal of a user's system. 50msec after the RESET signal rising edge the PPMC101C/102A is operative for initialization and operation command. The pulse width of the RESET signal must be no less than 2.5 µsec.*

## 2-3 $\overline{\text{CS}}$

*Input for chip select. To input the decorded signal from upper bits of ADDRESS. PPMC101C/102A is accessible at a low level 'O' on CS.*

## 2-4 $\overline{\text{RD}}$

*I/O read input which enables the master CPU to write data and status words from the PPMC101C/102A. The OUTPUT DATA BUS BUFFER or status register can be READ at a low level 'O' on $\overline{CS}$ and $\overline{RD}$.*

## 2-5 $\overline{\text{WR}}$

*I/O write input which enables the master CPU to write data and commands words to the PPMC101C/102A. Data on INPUT DATA BUS BUFFER can be written at a low level 'O' on $\overline{CS}$ and $\overline{RD}$.*

## 2-6 AO

*Address input used by the master processor to indicate whether the byte transfer is data or command as shown in the following table*

| Ao | $\overline{RD}$ | $\overline{WR}$ |
|---|---|---|
| 0 | Data Resister | Data Resister |
| 1 | Status Resister | Command Resister |

*Table 1*

## 2-7 SYNC

*Output signal which occurs once per execution of internal command in the PPMC101C/102A. It is also used to synchronize the single step operation. It is to be normally OPEN and used to check IC operation.*

## 2-8 DO-D7

*Tri-state, bidirectional DATA BUS BUFFER lines used to interface the PPMC101C/102A to an 8-bit master system data bus.*

## 2-9 $\overline{L1}$ - $\overline{L4}$, $\overline{CNP}$

*Inputs for external 'Limit' switches. Each signal is activated at a low level 'O'. Fig 2-2 shows the idea of 'Limit" switches.*

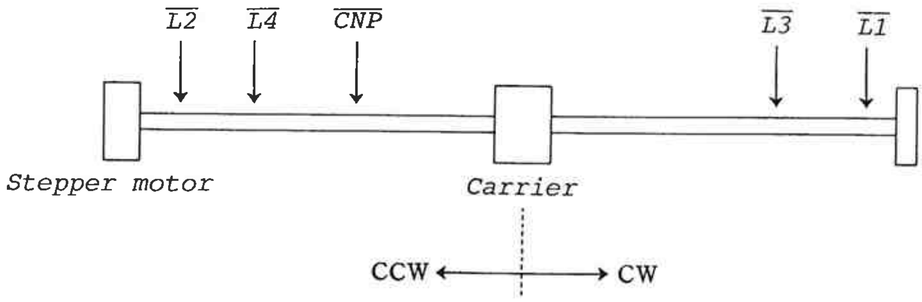



*Fig 2-2*

*L1, L2 :*

*These switches are set at a maximum limit position where the carrier does not move further in CCW or CW. The motor will stop immediately when the carrier moves to these points regardless of the operation command. The carrier will no longer move further in the same direction even when it receives a command to move in the same direction. The carrier will start to move in the opposite direction only when it receives the command to move in reverse.*

*L3, L4 :*

*These switches must be positioned between L1 and L2, at a minimum distance corresponding to the number of deceleration steps. The stepper motor begins to decelerate at these positions (L3 or L4) in order to stop inside of L1 or L2.*

*$\overline{CNP}$ :*

*Signal from $\overline{CNP}$ is used to establish a convenient reference point (Base point) with which the PPMC can monitor the position of the carrier. It does this by counting the number of steps in the data register. For example, in figure 2-2, in order to establish a convenient base point the command "move to base point" is used (see section 3-3-8). The motor will move the carrier to the position marked $\overline{CNP}$ and stop. Work can then proceed from this point.*

## 2-10 $\overline{\text{P-OUT}}$, CCW/$\overline{\text{CW}}$

*P-OUT is used for pulse output for other stepper motor driving modules without using PPMC phase output. It is useful for bipolar drive, switching drive and other special type of excitation method. It is recommended to use a decoder for CW or CCW pulse generation in combination with one-shot TIMER as shown in Fig 2-3 because driving module sometimes require 10 to 20 µsec pulse width. The signal from pulse output is a 5 µsec negative pulse and signal for direction is indicated by its level. In addition, these signals can be used for monitoring direction or number of pulses for rotation. CCW/$\overline{CW}$ can be activated only when $\overline{P\text{-}OUT}$ is active.*

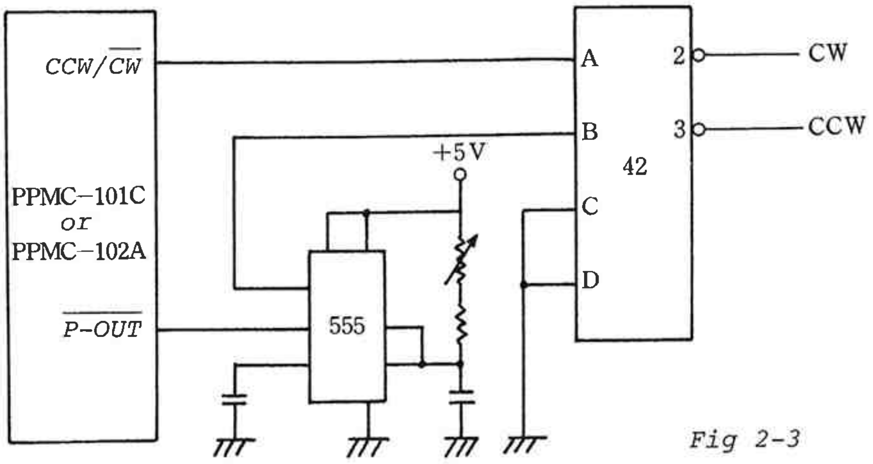



*Fig 2-3*

*P-OUT is always available as well, in use of any type of phase output. (see page 13. motor code 01, 10, 11)*

## 2-11 HOLD

*HOLD output is high 3 msec after motor stops, but it is active only when bit 5 of the initialization command is set. (see page 13)*

## 2-12 S1-S5

*Provides signal for motor excitation drive.*

| *Motor* | *Control* |
|---|---|
| *3 phase by* | *S1 - S3* |
| *4 " "* | *S1 - S4* |
| *5 " "* | *S1 - S5* |

*Fig 2-4 shows the form of output.*

*The logic can be interchanged, positive to negative logic, and visa versa. Typical circuit is shown in Fig 2-5.*

## EXCITATION PULSE OUTPUT

*2-phase excitation*

| | S1 | S2 | S3 |
|---|---|---|---|
| 1 | ■ | ■ | |
| 2 | | ■ | ■ |
| 3 | ■ | | ■ |

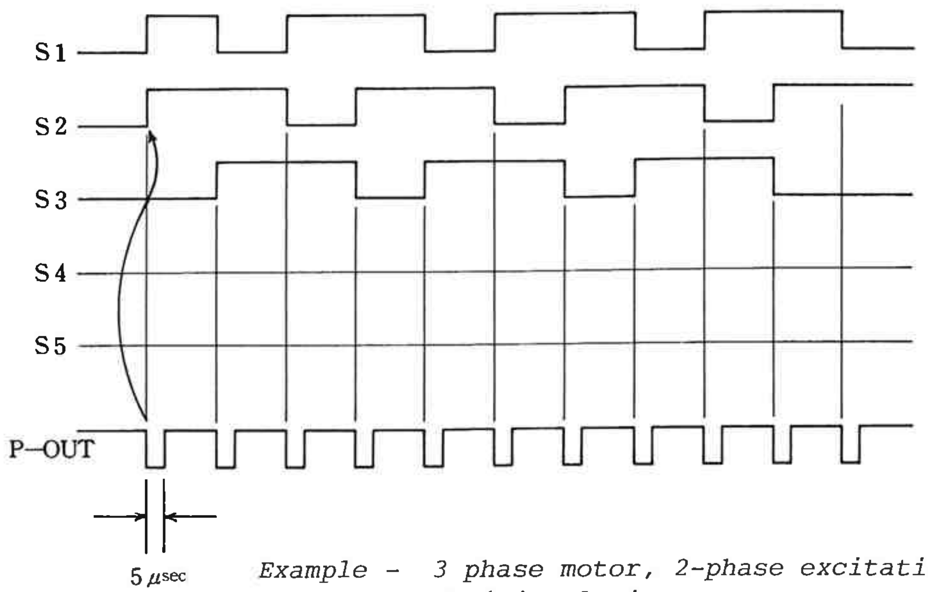
*(3-phase motor)*

| | S1 | S2 | S3 | S4 |
|---|---|---|---|---|
| 1 | ■ | ■ | | |
| 2 | | ■ | ■ | |
| 3 | | | ■ | ■ |
| 4 | ■ | | | ■ |

*(4-phase motor)*

| | S1 | S2 | S3 | S4 | S5 |
|---|---|---|---|---|---|
| 1 | ■ | ■ | | | |
| 2 | | ■ | ■ | | |
| 3 | | | ■ | ■ | |
| 4 | | | | ■ | ■ |
| 5 | ■ | | | | ■ |

*(5-phase motor)*




*Example - 3 phase motor, 2-phase excitation positive logic*

*Fig 2-4*

*1-2 phase excitation*

| | S1 | S2 | S3 |
|---|---|---|---|
| 1 | ■ | | |
| 2 | ■ | ■ | |
| 3 | | ■ | |
| 4 | | ■ | ■ |
| 5 | | | ■ |
| 6 | ■ | | ■ |

*(3-phase motor)*

| | S1 | S2 | S3 | S4 |
|---|---|---|---|---|
| 1 | ■ | | | |
| 2 | ■ | ■ | | |
| 3 | | ■ | | |
| 4 | | ■ | ■ | |
| 5 | | | ■ | |
| 6 | | | ■ | ■ |
| 7 | | | | ■ |
| 8 | ■ | | | ■ |

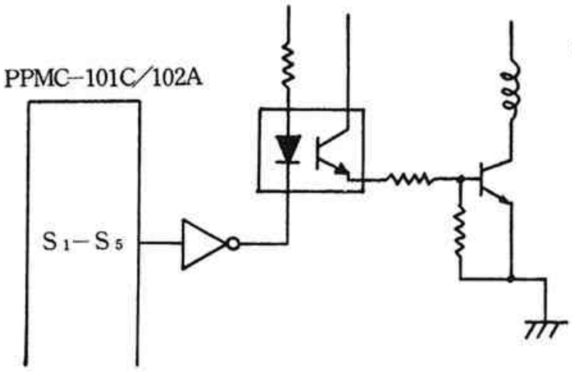
*(4-phase motor)*

*2-3 phase excitation*

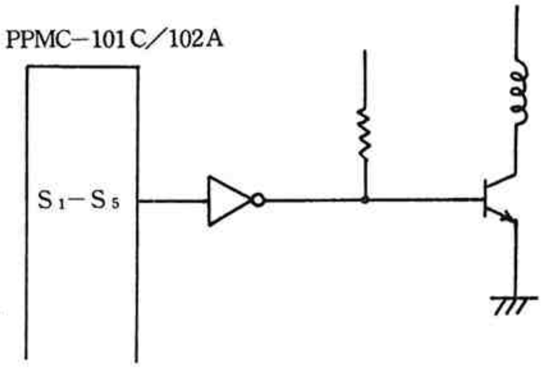
| | S1 | S2 | S3 | S4 | S5 |
|---|---|---|---|---|---|
| 1 | ■ | ■ | | | |
| 2 | ■ | ■ | ■ | | |
| 3 | | ■ | ■ | | |
| 4 | | ■ | ■ | ■ | |
| 5 | | | ■ | ■ | |
| 6 | | | ■ | ■ | ■ |
| 7 | | | | ■ | ■ |
| 8 | ■ | | | ■ | ■ |
| 9 | ■ | | | | ■ |
| 10 | ■ | ■ | | | ■ |

*(5-phase motor)*

*Output logic level can be switched by using positive or negative logic as shown in Fig. 2-5.*




*Output*
*Positive logic convention*




*Output*
*Negative logic convention*

*Fig. 2-5*

## 2-13 $\overline{INT}$

*Interrupt request is assertive 'O' when motor stops. $\overline{INT}$ can be cleared by reading the finish STATUS. This figure is not an open collector and OPEN COLLECTOR BUFFER is required as shown in Fig 2-6, when a multiple INTERUPT is expected.*

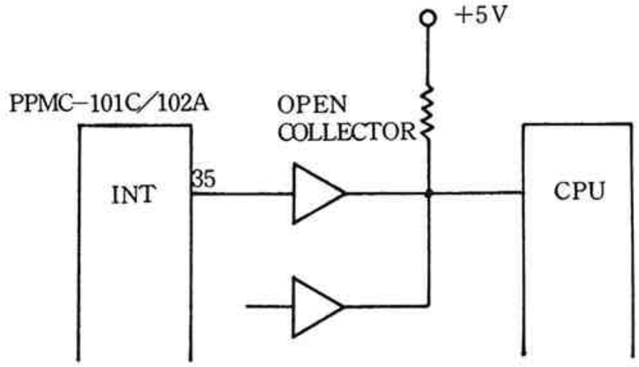



*Fig 2-6*

## 2-14 MON

*When motor on input is 'O', PPMC does not output driving pulse. An example of an application is indicated in Fig 2-7, in which a thermal relay on the motor is used to protect overheating. MON input is ignored during operation of PPMC, and should be checked only before motor operation.*

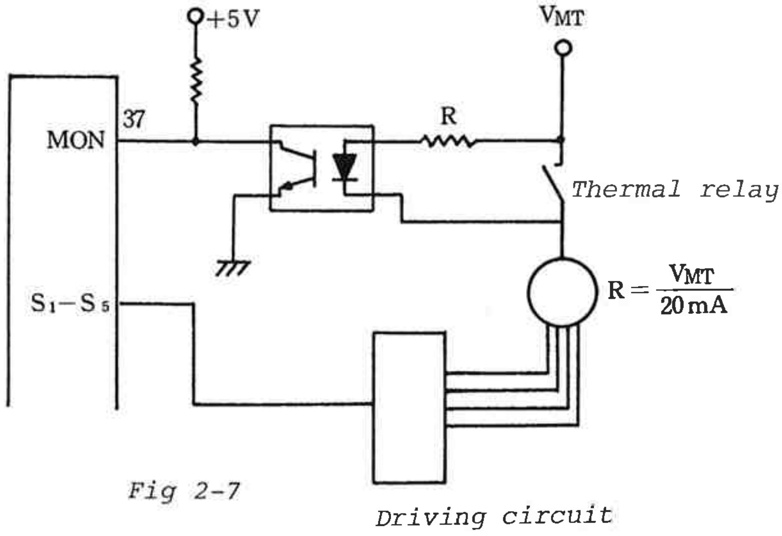



*Fig 2-7*

## 2-15 CLOCK-external clock

*Basic signal to control speed of the stepper motor. The speed can be controlled between 400pps and 5K pps by the 100KHz clock input to PPMC101C and between 800pps and 10K pps by 200KHz clock input to PPMC102A. The clock frequency must be below 1/45 of X1, X2 clock. For example, when 6MHz X-tal is applied for X1 and X2, external clock input must be less than 133KHz (in case 11MHz is applied, external clock must be less than 244KHz). High level of the clock pulse must be more than 500 nsec.(250 nsec for 11MHz)*

# 3. COMMUNICATION BETWEEN PPMC AND MASTER CPU

*The communication between PPMC and master CPU consists of following 3 types of modes :*

*(1) Initialization*

*It designates type of motor, method of excitation, data for acceleration/deceleration and other parameters (see page 13 for details). After power 'ON', initialization is needed before operation command. Note : Some parameters cannot be changed once it is set. Re-initialization is not possible during operation.*

*(2) Operation Command*

*8 kinds of operation commands are available for stepper motor. The length of data to follow depends on the command.*

*(3) Register for PPMC*

*After completion of (2), master CPU reads the cause of operation finish, status of input/output terminal, and the number of remaining pulse.*

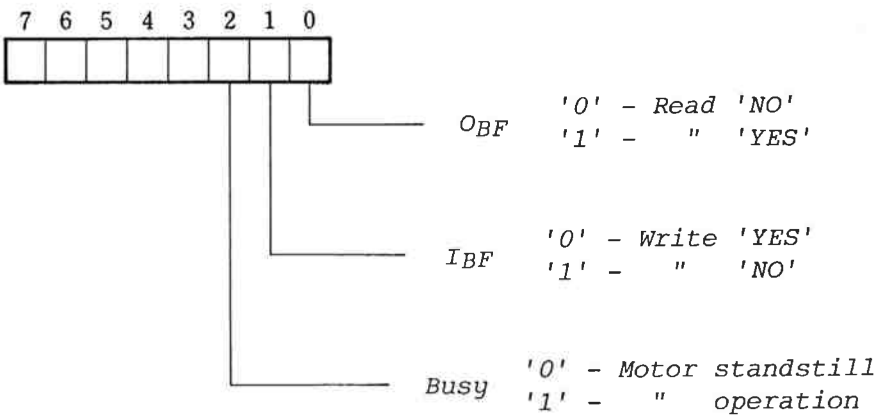
## 3–1 Register for PPMC

*2 read only registers, and 2 write only registers are accessible to the uses.*

| $\overline{CS}$ | $A_0$ | $\overline{RD}$ | $\overline{WR}$ | |
|---|---|---|---|---|
| 1 | × | × | × | DISABLE |
| 0 | 0 | 0 | 1 | READ DATA |
| 0 | 1 | 0 | 1 | READ STATUS |
| 0 | 0 | 1 | 0 | WRITE DATA |
| 0 | 1 | 1 | 0 | WRITE COMMAND |

*Table 3-1*

### *3-1-1 Status Register*



# COMMAND TABLE

| | | | COMMAND DATA | FUNCTION |
|---|---|---|---|---|
| INITIALIZATION | | 1<br>2<br>3<br>4<br>5 | 0 0<br>Self-starting pulse rate<br>High speed pulse rate<br>Accelerating/Decelerating pulse rate | |
| OPERATING COMMAND | Emergency Stop | 1 | 0 1 0 0 0 |  |
| | Decelerating Stop | 1 | 0 1 0 0 1 |  |
| | Single Step | 1 | 0 1 0 1 0 |  |
| | Acceleration/ Deceleration | 1<br>2<br>3<br>4 | 0 1 0 1 1<br><br>Number of operating step |  |
| | Constant speed operation | 1<br>2<br>3<br>4<br>5 | 0 1 1 0 0<br>Constant speed pulse rate<br><br>Number of operating step |  |
| | To move until the limit at constant speed | 1<br>2 | 0 1 1 0 1<br>Constant speed pulse rate |  |
| | To move until high speed limit | 1 | 0 1 1 1 0 |  |
| | To move to the base point | 1<br>2 | 0 1 1 1 1<br>Contant speed pulse rate |  |
| READ REGISTER | Finish Data | 1 | 1 0 0 0 0 0 0 0 | To read data for reason of FINISH, etc. ............ 1 byte |
| | Input signal | 1 | 1 0 0 0 0 0 0 1 | To read data for limit switch, etc. ............... 1 byte |
| | Output signal | 1 | 1 0 0 0 0 0 1 0 | To read data for motor phase output and direction ... 1 byte |
| | Remaining step numbers | 1 | 1 0 0 0 0 0 1 1 | To read remaining number of steps ................. 3 byte |