RevNo	Revision note	Date	By	Checked
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CORE–BUSS [1]
C–BUSS [1,3,4]
Z–BUSS
CONTROL [1,3,4,5,6,7,8,9,10,11]
FUNCTIONS [3,4,5,6,7,8,9,10]

T
AC0
2GR36–VE
K8
2TR16
2TR11 2G210
ZAC0
ZAC0

T
Z1
F4
AC
K9
2TR22
2TR26 2G210
ZAC1
ZAC1

T
F4
F5
AC
K10
2TR38
2TR42 2G210
ZAC2
ZAC2

T
F4
F5
AC
K11
2TR7
2TR3 2G210
ZAC3
MP5
ZAC3

–13,5V [1,2]
40R

T
READ
Z4
K16
2TR27
2TR29 2G210
S4L
COM2
S4L

T
WRITE
Z4
K17
2TR23
2TR28 2G210
S4S
S4S

T
READ
Z4
K18
2TR36
2TR32 2G210
S4L
S4L

T
WRITE
Z4
K19
2TR43
2TR39 2G210
S4S
S4S

T
WRITE
C1
K24
2TR13
2TR9 2G210
BL1
MP7
40R
COM2
BL1

T
WRITE
C8
K25
2TR5
2TR1 2G210
BL8
MP8
40R
BL8

T
MRS
K6
2TR31
2TR35 2G210
ZMR
ZMR

T
MDS
K7
2TR21
2TR15 2G210
ZMD
ZMD

T
Z1
Z2
K20
2TR40
2TR37 2G210
SS1
SS1

T
Z1
Z2
K21
2TR24
2TR19 2G210
SS2
SS2

T
Z1
Z2
K22
2TR18
2TR14 2G210
SS3
SS3

T
Z1
Z2
K23
2TR33
2TR30 2G210
SS4
MP6
SS4

–13,5V [1,2]
40R

T
READ
Z8
K12
2TR6
2TR2 2G210
Z8L
COM2
Z8L

T
WRITE
Z8
K13
2TR20
2TR44 2G210
Z8S
Z8S

T
READ
Z8
K14
2TR17
2TR12 2G210
Z8L
Z8L

T
WRITE
Z8
K15
2TR8
2TR4 2G210
Z8S
Z8S

Memory timing

K(MS)
S1
EN
2C33
2GR61
T
SET
Q
TR34
TR41
4uS
N1
N2
T
+12V
2W108 50K

Negative logic referenced to 0V – Logical 1 = –12v, logical 0 = 0v

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Pcb Dwg # =			Scale	Nts
	Name	Date	Sheet	2
Drawn	MD Hatch	9/10/2009	Next Sheet	3
Checked	–	–	Drawing Number	Soemtron 220 Logic A2 Issue A

Title: Soemtron ETR 220 Calculator
#2 – Core Memory Drivers
Logic Diagram