RevNo	Revision note	Date	By	Checked
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CORE-BUSS [1]
C-BUSS [1,7,8,14]
Z-COUNTER [3,4,5,6]
CONTROL [1,3,4,5,6,7,8,9,10,11,12,14,15,16]
FUNCTIONS [3,4,5,6,7,8,9,10,11,12,15]

ZAC0: T, AC0, 2GR36-VE → K8 → 2TR16 → 2TR11 2G210 → ZAC0
ZAC1: T, $\overline{Z1}$, F4, AC → K9 → 2TR22 → 2TR26 2G210 → ZAC1
ZAC2: T, $\overline{F4}$, F5, AC → K10 → 2TR38 → 2TR42 2G210 → ZAC2
ZAC3: T, F4, F5, AC → K11 → 2TR7 → 2TR3 2G210 → ZAC3
MP5; −13.5V [1,2] via 40R

$\overline{S4L}$: T, READ, $\overline{Z4}$ → K16 → 2TR27 → 2TR29 2G210 → COM2
$\overline{S4S}$: T, WRITE, $\overline{Z4}$ → K17 → 2TR23 → 2TR28 2G210 → COM2
S4L: T, READ, Z4 → K18 → 2TR36 → 2TR32 2G210 → S4L
S4S: T, WRITE, Z4 → K19 → 2TR43 → 2TR39 2G210 → S4S

BL1: T, WRITE, C1 → K24 → 2TR13 → 2TR9 2G210 → COM2; MP7; 40R → BL1
BL8: T, WRITE, C8 → K25 → 2TR5 → 2TR1 2G210 → COM2; MP8; 40R → BL8
ZMR: T, MRS → K6 → 2TR31 → 2TR35 2G210 → ZMR
ZMD: T, MDS → K7 → 2TR21 → 2TR15 2G210 → ZMD

SS1: T, Z1, $\overline{Z2}$ → K20 → 2TR40 → 2TR37 2G210 → SS1
SS2: T, $\overline{Z1}$, Z2 → K21 → 2TR24 → 2TR19 2G210 → SS2
SS3: T, Z1, Z2 → K22 → 2TR18 → 2TR14 2G210 → SS3
SS4: T, $\overline{Z1}$, $\overline{Z2}$ → K23 → 2TR33 → 2TR30 2G210 → SS4
MP6; −13.5V [1,2] via 40R

$\overline{Z8L}$: T, READ, $\overline{Z8}$ → K12 → 2TR6 → 2TR2 2G210 → COM2
$\overline{Z8S}$: T, WRITE, $\overline{Z8}$ → K13 → 2TR20 → 2TR44 2G210 → COM2
Z8L: T, READ, Z8 → K14 → 2TR17 → 2TR12 2G210 → Z8L
Z8S: T, WRITE, Z8 → K15 → 2TR8 → 2TR4 2G210 → Z8S

Memory timing

K(MS), S1 → EN → 2C33 → 2GR61 → T SET Q, TR34, TR41 4uS $\overline{Q}$ → N1 → N2 → T, $\overline{T}$
+12V; 2W108 50K

Negative logic referenced to 0V – Logical 1 = −12v, logical 0 = 0v

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Pcb Dwg # =			Scale	Nts
	Name	Date	Sheet	2
Drawn	MD Hatch	3/02/2021	Next Sheet	3
Checked	–	–	Drawing Number	Soemtron 222 Logic A2 Issue A

Title: Soemtron ETR 222 Calculator
#2 – Core Memory Drivers
Logic Diagram